WHAT IS CLAIMED IS:

1. A method of laminating a circuit board comprising the steps of:

providing a first layer having a substrate of dielectric material having a conductive signal plane, said signal plane having at least one surface with a first roughness;

forming said signal plane into signal lines and lands;

thereafter selectively roughening at least a portion of said first surface to form a second surface having a second roughness greater than said first roughness;

providing a second layer comprised of a voltage plane as a single sheet of foil or disposed on a substrate of dielectric material; and laminating said first layer to said second layer with a sticker sheet therebetween to form a composite structure; said signal plane and said voltage plane being oriented toward each other;

said composite structure being formed with plated through holes surrounded by said lands.

2. The invention as defined in claim 1 wherein said portion of said second surface of said signal plane includes said lands surrounding said plated through holes.

3. The invention as defined in claim 2 wherein said roughness of said at least one surface of said second portion of said signal plane has an R_z value greater than about 3 microns.

4. The invention as defined in claim 2 wherein the roughness of said at least one surface of said signal plane has an Rz value of less than about 1 micron.

5. The invention as defined in claim 2 wherein the roughness of said at least one surface of said first portion of said signal plane has an R_z value less than about 1 micron, and the roughness of said second surface of said signal plane has an R_z value greater than about 3 microns.

6. The invention as defined in claim 2 wherein said first portion of said signal plane has a plurality of said surfaces with a first roughness.

7. The invention as defined in claim 6 wherein said plurality of surfaces of said first portion of said signals plane include at least three surfaces.

8. The invention as defined in claim 1 wherein said voltage plane has a first portion with at least one surface with a first surface roughness aligned with the first portion of said signal lines, and a second portion having a second surface with a surface roughness greater than the surface roughness of said at least one surface of said first portion thereof.

9. The invention as defined in claim 8 wherein said first portion of said surface of said voltage plane has an R_z value surface roughness of less than about 1 micron

and said second portion of said surface of said voltage plane has an R_z value of greater than about 3 microns.

10. The invention as defined in claim 1 wherein said roughened surfaces are roughened by treating the copper surface with an oxide or an oxide replacement process, or having plated thereon zinc, brass, nickel or chrome.

11. The invention a defined in claim 1 wherein said surface having said second roughness is created by applying a photoresist material to said voltage plane, then exposing and developing said photoresist to reveal the surface to have said second roughness, then treating said second surface to provide the desired surface roughness, then removing the photoresist.

12. The invention as defined in claim 1 wherein said surface having said second roughness is created by,

applying a masking material to all of the areas of said voltage plane that are not to have said second roughness,

then roughening those areas to have said second roughness.

13. The invention as defined in claim 8 wherein said roughened surfaces are roughened by treating the copper surface with an oxide or an oxide replacement process, or having plated thereon zinc, brass, nickel or chrome.

14. The invention a defined in claim 8 wherein said surface having said second roughness is created by applying a photoresist material to said voltage plane, then exposing and developing said photoresist to reveal the surface to have said second roughness, then treating said second surface to provide the desired surface roughness, then removing the photoresist.

15. The invention as defined in claim 8 wherein said surface having said second roughness is created by,

applying a masking material to all of the areas of said voltage plane that are not to have said second roughness,

then roughening those areas to have said second roughness.